REMARKS

Applicants acknowledge, with appreciation, the Examiner's allowance of Claims 14 - 19 and the indication of the allowability of Claims 2, 12 and 13, if rewritten in independent form.

Accordingly, Claim 2 has been canceled and Claim 1 has been amended to include the limitations of Claim 2. Claims 12 and 13 have also been canceled and rewritten as new Claims 21 and 22 so as to include all of the limitations of Claims 1, 12 and 13. Allowed Claim 14 has been amended to change "first" to "reverse" in para. 6 to correct an inconsistency in claim recitation.

The specification has been amended at pages 9 and 12 so that "via 22" reads as "via pads 22" to correct an obvious error.

The Examiner has rejected Claims 1 and 3 - 11 under 35 USC 103(a) as being unpatentable over Han (US6,593,184B2).

In this rejection, the Examiner attempts to read Claims 1 and 3 - 11 on Han except for the "protective overcoat layer over the interconnection structure" limitation. For this limitation, the Examiner asserts "it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form a protective overcoat layer over the interconnection structure 45 because the protective overcoat would protect the interconnection structure during the bonding process".

Applicants do not agree with the conclusion of the Examiner. Firstly, if the interconnection structure 45 on wafer 40 of Han were covered with a protective overcoat,

as suggested by the Examiner, then the interconnection structure 45 would not make electrical contact to pad 39 on wafer 31, as intended by Han. This fact makes clear the point that wafer 40 is not intended to be temporarily attached to wafer 31 for processing purposes, but rather is attached to form a stacked device, as pointed out by Han in Col. 2.

In this regard, Claim 1 calls for "forming a protective overcoat layer over the interconnection structure" and then "forming a temporary bond between the protective overcoat layer of the SBP and a wafer holder" (emphasis added). It is clear that Han does not form a temporary bond between wafer 40 and wafer 39. Applicants' temporary bond is just that - temporary. Applicants' protective overcoat does not interfere with any interconnections because connection is made from the backside by way of the through via holes.

It is also clear that wafer 31 would not be considered, by one skilled in the art, to be a "wafer holder". It would not be reasonable to use a "wafer" as a temporary "wafer holder" when less costly alternatives are clearly available.

Accordingly, it would not be obvious to form a protective overcoat layer over the interconnection structure of Han because such would render Han inoperative for its intended purposes. Clearly, there would be no motivation for one skilled in the art to form such protective overcoat layer over the interconnection structure 45 of Han, or to form a temporary bond between such protective overcoat layer and wafer 31.

It is also clear that the Examiner has not addressed the limitations of dependent Claims 3 - 11. For example, Claim 3 calls for "forming metal capture structures over the first surface". Han fails to show such structure. Claim 4 calls for forming the "metal capture structures" and "then forming the interconnection structure over the first surface

and the metal capture structures and then forming the protective overcoat layer" (emphasis added). Again, Han clearly fails to teach such structure.

Claim 5 goes even further in calling for "forming the metal capture structures", then "forming the interconnection structure over the first surface and metal capture structures", then "forming the protective overcoat layer" then "thinning" and finally "forming the VSTV holes through the UTSW ... reaching down to form VSTV bases on the metal capture structures" (emphasis added). Again, Han clearly fails to suggest or teach such structure.

Claim 6 adds a further limitations over Claim 5 calling for "then forming a dielectric layer over the surface of the wafer leaving the bottoms of the VSTV holes clear over the metal capture structures" and "then forming metal pads in the VSTV holes in contact with the metal capture structures". Again, Han clearly fails to teach or suggest such structure.

Claim 7 calls for the additional step over Claim 6 of the "forming metal joining structures on the metal pads". Again, Han fails to teach or suggest such structure. Claims 8 - 11 similarly recite limitations not found in Han.

Although Applicants believe that Claims 1 and 3 - 11, as set forth, are clearly patentable over Han, in order to expedite the issuance of Claim 1, as amended, Claims 14 - 19 and 21 and 22, Applicants have canceled the rejected Claims. Thus, rejected Claims 2 - 13 and withdrawn Claim 20 have been canceled putting the application, prima facia, in condition for allowance.

Accordingly, Applicants respectfully request the Examiner to allow the claims as now presented, and pass the case to issue.

Respectfully submitted,

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